AMENDMENTS TO THE CLAIMS

Please amend claims 16-17, 22-23, 30-31 and 37-38 as follows:

1. (Original) A CMOS image sensor comprising:

a semiconductor structure, wherein the semiconductor structure includes a unit pixel area and a pad area;

a metal line formed on the pad area, wherein a portion of the metal line is exposed;

a passivation layer formed on the unit pixel area and on the metal line such that the exposed portion of the metal line is left exposed;

a planarized photoresist formed on a portion of the passivation layer;

a micro-lens formed on a portion of the planarized photoresist; and

an oxide layer formed on the micro-lens, the photoresist and the passivation layer such that the exposed portion is left exposed.

2. (Original) The CMOS image sensor as recited in claim 1, wherein the oxide layer is formed at a temperature of 150°C to 200°C.

3. (Original) The CMOS image sensor as recited in claim 2, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

4. (Original) The CMOS image sensor as recited in claim 1, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

5. (Original) The CMOS image sensor as recited in claim 1, wherein the passivation layer includes a nitride layer and a second oxide layer.

6. (Original) The CMOS image sensor as recited in claim 4, further comprising an anti-reflection layer formed on the metal line such that the exposed portion is left exposed.

7. (Original) The CMOS image sensor as recited in claim 1, further comprising an anti-reflection layer formed on the metal line such that the exposed portion is left exposed.

8. (Original) A method for fabricating a CMOS image sensor, comprising the steps of:

a) providing a semiconductor structure, wherein the semiconductor structure includes a metal line formed on an upper portion of the semiconductor structure;

b) forming a passivation layer on the metal line;

c) forming a planarized photoresist on a portion of the passivation layer;

d) forming a micro-lens on a portion of the planarized photoresist;

e) forming an oxide layer on the micro-lens, the photoresist and the passivation layer; and

f) forming a pad open mask and etching the oxide layer and the passivation layer to expose a portion of the metal line.

9. (Original) The method as recited in claim 8, wherein the oxide layer is formed at a temperature of 150°C to 200°C.

10. (Original) The method as recited in claim 9, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

11. (Original) The method as recited in claim 8, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

12. (Original) The method as recited in claim 8, wherein the passivation layer includes a nitride layer and a second oxide layer.

13. (Original) The method as recited in claim 12, further comprising the step of forming an anti-reflection layer on the metal line.

14. (Original) The method as recited in claim 13, wherein the exposed portion of the metal line is not covered by the anti-reflection layer.

15. (Original) The method as recited in claim 8, further comprising the step of forming an anti-reflection layer on the metal line.

16. (Currently amended) A CMOS image sensor comprising:

a semiconductor structure, wherein the semiconductor structure includes a unit pixel area and a pad area;

a metal line formed over the pad area;

a planarized photoresist formed over a portion of the unit pixel area;

a micro-lens formed on a portion of the planarized photoresist; and

an oxide layer formed to cover a resulting structure ~~including the micro-lens and the photoresist~~ in the unit pixel area and the pad area.

17. (Currently amended) The CMOS image sensor as recited in claim 16, further comprising:

a passivation layer formed on the unit pixel area and the ~~pad area~~ metal line: and

an opening portion exposing a portion of the metal line by passing through the oxide layer, ~~the planarized photoresist~~ and the passivation layer.

18. (Original) The CMOS image sensor as recited in claim 16, wherein the oxide layer is formed at a temperature of 150°C to 200°C.

19. (Original) The CMOS image sensor as recited in claim 18, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

20. (Original) The CMOS image sensor as recited in claim 17, wherein the passivation layer includes a nitride layer and a second oxide layer.

21. (Original) The CMOS image sensor as recited in claim 20, further comprising an anti-reflection layer formed on the metal line such that the exposed portion is left exposed.

22. (Currently amended) A method of fabrication a CMOS image sensor, comprising the steps of:

a) providing a semiconductor structure, wherein the semiconductor structure includes a metal line formed in an upper portion of the semiconductor structure;

b) forming a planarized photoresist over a portion of the semiconductor structure;

c) forming a micro-lens on a portion of the planarized photoresist; and

d) forming an oxide layer to cover a resulting structure ~~including the micro-lens~~ in the unit pixel area and the pad area.

23. (Original) The method as recited in claim 22, further comprising forming a passivation layer on the semiconductor structure before the step b).

24. (Currently amended) The method as recited in claim 23, further comprising e) forming an opening portion to expose a portion of the metal line by selectively etching the oxide layer~~, the planarized photoresist~~ and the passivation layer.

25. (Original) The method as recited in claim 22, wherein the oxide layer is formed at a temperature of 150°C to 200°C.

26. (Original) The method as recited in claim 25, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

27. (Original) The method as recited in claim 23, wherein the passivation layer includes a nitride layer and a second oxide layer.

28. (Original) The method as recited in claim 24, further comprising forming an anti-reflection layer on the metal line before forming the passivation layer.

29. (Original) The method as recited in claim 28, wherein the portion of the metal line exposed through the opening portion is not covered by the anti-reflection layer.

30. (Currently amended) A CMOS image sensor comprising:

a semiconductor structure, wherein the semiconductor structure includes a unit pixel area and a pad area;

a metal line formed on the pad area;

a micro-lens formed over a portion of the ~~the~~ unit pixel area; and

an oxide layer formed to cover a resulting structure ~~including the micro-lens~~ in the unit pixel area and the pad area.

31. (Currently amended) The CMOS image sensor as recited in claim 30, further comprising:

a passivation layer formed on the unit pixel area and on the metal line such:

a planarized photoresist formed on a portion of the passivation layer; and

an opening portion exposing a portion of the metal line by passing through the oxide layer~~, the planarized photoresist~~ and the passivation layer.

32. (Original) The CMOS image sensor as recited in claim 31, wherein the planarized photoresist includes a color filter.

33. (Original) The CMOS image sensor as recited in claim 31, wherein the oxide layer is formed at a temperature of 150°C to 200°C.

34. (Original) The CMOS image sensor as recited in claim 33, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

35. (Original) The CMOS image sensor as recited in claim 34, wherein the passivation layer includes a nitride layer and a second oxide layer.

36. (Original) The CMOS image sensor as recited in claim 31, further comprising an anti-reflection layer formed on the metal line such that the exposed portion is left exposed.

37. (Currently amended) A method of fabrication a CMOS image sensor, comprising:

a) providing a semiconductor structure, wherein the semiconductor structure includes a metal line formed on an upper portion of the semiconductor structure;

b) forming a micro-lens over a portion of the semiconductor structure; and

c) forming an oxide layer overlaying a resulting structure ~~including the micro-lens~~ in the unit pixel area and the pad area.

38. (Currently amended) The method as recited in claim 37, further comprising:

forming a passivation layer on the unit pixel area and the metal line;

forming a planarized photoresist on a portion of the passivation layer; and

forming an opening portion to expose a portion of the metal line by selectively etching the oxide layer~~, the planarized photoresist~~ and the passivation layer.

39. (Original) The method as recited in claim 37, wherein the oxide layer is formed at a temperature of 150°C to 200°C.

40. (Original) The method as recited in claim 39, wherein the oxide layer is formed to a thickness of 3000 Å to 10000 Å.

41. (Original) The method as recited in claim 38, wherein the passivation layer includes a nitride layer and a second oxide layer.

42. (Original) The method as recited in claim 38, further comprising forming an anti-reflection layer on the metal line before forming the passivation layer.

43. (Original) The method as recited in claim 42, wherein the portion of the metal line exposed through the opening portion is not covered by the anti-reflection layer.